Refine Search

Search Results -

Terms	Documents
L8 and ((share$2 NEAR3 copy) or (exclusive NEAR2 copy))	9

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L10

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, October 01, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L10	L8 and ((share$2 NEAR3 copy) or (exclusive NEAR2 copy))	9	L10
L9	L8 and (state adj machine).ab.	3	L9
L8	L7 and process$4	22	L8
L7	L6 and (multi$2node NEAR6 computer)	22	L7
L6	(state adj machine)	35557	L6
L5	l4 and (state adj2 machine)	0	L5
L4	((multi$2node NEAR6 computer) NEAR5 (process$5 NEAR4 (multiple or plural or several)))	6	L4
L3	(l1 or l2) and ((multi$2node NEAR6 computer) NEAR5 (process$5 NEAR4 (multiple or plural or several)))	1	L3
L2	g06f 12/00	602221	L2
L1	g06f 12/08	602252	L1

END OF SEARCH HISTORY

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 9 of 9 returned.

☐ 1. Document ID: US 20040148472 A1

Using default format because multiple data bases are involved.

L10: Entry 1 of 9 File: PGPB Jul 29, 2004

PGPUB-DOCUMENT-NUMBER: 20040148472
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040148472 A1

TITLE: Multiprocessor cache coherence system and method in which processor nodes and input/output nodes are equal participants

PUBLICATION-DATE: July 29, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Barroso, Luiz A.	Mountain View	CA	US	
Gharachorloo, Kourosh	Menlo Park	CA	US	
Nowatzyk, Andreas	San Jose	CA	US	
Ravishankar, Mosur K.	Mountain View	CA	US	
Stets, Robert J. JR.	Palo Alto	CA	US	

US-CL-CURRENT: 711/141; 711/145

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 2. Document ID: US 20020124144 A1

L10: Entry 2 of 9 File: PGPB Sep 5, 2002

PGPUB-DOCUMENT-NUMBER: 20020124144
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020124144 A1

TITLE: Scalable multiprocessor system and cache coherence method implementing store-conditional memory transactions while an associated directory entry is encoded as a coarse bit vector

PUBLICATION-DATE: September 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47

Gharachorloo, Kourosh	Menlo Park	CA	US
Barroso, Luiz Andre	Mountain View	CA	US
Ravishankar, Mosur K.	Mountain View	CA	US
Stets, Robert J.	Palo Alto	CA	US
Scales, Daniel J.	Mountain View	CA	US

US-CL-CURRENT: 711/145; 711/144

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 3. Document ID: US 20020010840 A1

L10: Entry 3 of 9 File: PGPB Jan 24, 2002

PGPUB-DOCUMENT-NUMBER: 20020010840
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020010840 A1

TITLE: Multiprocessor cache coherence system and method in which processor nodes and input/output nodes are equal participants

PUBLICATION-DATE: January 24, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Barroso, Luiz A.	Mountain View	CA	US	
Gharachorloo, Kourosh	Menlo Park	CA	US	
Nowatzyk, Andreas	San Jose	CA	US	
Ravishankar, Mosur K.	Mountain View	CA	US	
Stets, Robert J. JR.	Palo Alto	CA	US	

US-CL-CURRENT: 711/141; 711/117

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 4. Document ID: US 6766360 B1

L10: Entry 4 of 9 File: USPT Jul 20, 2004

US-PAT-NO: 6766360
DOCUMENT-IDENTIFIER: US 6766360 B1

TITLE: Caching mechanism for remote read-only data in a cache coherent non-uniform memory access (CCNUMA) architecture

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 5. Document ID: US 6748498 B2

L10: Entry 5 of 9 File: USPT Jun 8, 2004

US-PAT-NO: 6748498
DOCUMENT-IDENTIFIER: US 6748498 B2

TITLE: Scalable multiprocessor system and cache coherence method implementing store-conditional memory transactions while an associated directory entry is encoded as a coarse bit vector

☐ 6. Document ID: US 6675265 B2

L10: Entry 6 of 9 File: USPT Jan 6, 2004

US-PAT-NO: 6675265
DOCUMENT-IDENTIFIER: US 6675265 B2

TITLE: Multiprocessor cache coherence system and method in which processor nodes and input/output nodes are equal participants

☐ 7. Document ID: US 6182089 B1

L10: Entry 7 of 9 File: USPT Jan 30, 2001

US-PAT-NO: 6182089
DOCUMENT-IDENTIFIER: US 6182089 B1

TITLE: Method, system and computer program product for dynamically allocating large memory pages of different sizes

☐ 8. Document ID: US 6141692 A

L10: Entry 8 of 9 File: USPT Oct 31, 2000

US-PAT-NO: 6141692
DOCUMENT-IDENTIFIER: US 6141692 A

TITLE: Directory-based, shared-memory, scaleable multiprocessor computer system having deadlock-free transaction flow sans flow control protocol

☐ 9. Document ID: US 6041376 A

L10: Entry 9 of 9 File: USPT Mar 21, 2000

US-PAT-NO: 6041376
DOCUMENT-IDENTIFIER: US 6041376 A
** See image for Certificate of Correction **

TITLE: Distributed shared memory system having a first node that prevents other nodes from accessing requested data until a processor on the first node controls the requested data

Terms	Documents
L8 and ((share$2 NEAR3 copy) or (exclusive NEAR2 copy))	9

Refine Search

Search Results -

Terms	Documents
L18 and ((invalidate NEAR1 (request$2 or message$1)) NEAR20 ((share$2 NEAR3 copy) or (exclusive NEAR3 copy)))	0

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L20

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, October 01, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L20	L18 and ((invalidate NEAR1 (request$2 or message$1)) NEAR20 ((share$2 NEAR3 copy) or (exclusive NEAR3 copy)))	0	L20
L19	L18 and (multi$2node NEAR6 computer)	1	L19
L18	L17 and (state adj machine)	1342	L18
L17	g06f 12/08	602252	L17
L16	L10 and ((invalidate NEAR1 (request$2 or message$1)) NEAR20 ((share$2 NEAR3 copy) or (exclusive NEAR3 copy)))	2	L16
L15	L10 and (invalidate NEAR1 (request$2 or message$1))	23	L15
L14	L10 and (invalidate NEAR2 (request$2 or message$1))	23	L14
L13	L10 and (invalidate NEAR5 (request$2 or message$1))	50	L13
L12	L10 and (invalidate NEAR12 (request$2 or message$1))	50	L12
L11	L10 and invalidate	58	L11

L10	L8 and (cach$6 adj line)	61	L10
L9	L8 and (cach$6 adj2 line)	61	L9
L8	L6 and (home adj2 node)	61	L8
L7	l3 and L6	0	L7
L6	L1 and ((share$2 NEAR3 copy) or (exclusive NEAR3 copy))	221	L6
L5	L4 and ((share$2 NEAR3 copy) or (exclusive NEAR3 copy))	0	L5
L4	l1 and L3	10	L4
L3	g06f 13/364	602161	L3
L2	L1 and (multi$2node NEAR6 computer)	14	L2
L1	(state adj machine) and (share$2 adj memory)	2054	L1

END OF SEARCH HISTORY